Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

Claim 1 **(Currently Amended)**: A method for programming a group of at least one flash memory cell of an array, comprising:

A. performing a first pass of program verify and programming steps until each flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level after the first pass is completed; and

B. performing, after the first pass is completed, a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level.

Claim 2 **(Previously Presented)**: The method of claim 1, wherein the step A comprises a loop of the following steps:

determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step; and

generating a programming pulse for the flash memory cell of the group that has not attained substantially X% of the program verify level, during the programming step.

Claim 3 **(Previously Presented)**: The method of claim 1, wherein the step B comprises a loop of the following steps:

determining whether a flash memory cell of the group has not attained substantially the

program verify level, during the program verify step; and

generating a programming pulse for the flash memory cell of the group that has not attained the program verify level, during the programming step.

Claim 4 **(Previously Presented)**: The method of claim 1, wherein the group includes a plurality of flash memory cells to be programmed to multi-level threshold voltages, the method further comprising:

performing the first pass of program verify and programming steps until each flash memory cell of a first sub-group of the group attains a threshold voltage that is at least Y% of a first program verify level but less than the first program verify level, and until each flash memory cell of a second sub-group of the group attains a threshold voltage that is at least Z% of a second program verify level but less than the second program verify level; and

performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second program verify level.

Claim 5 **(Previously Presented)**: The method of claim 4, wherein (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to a higher of the first and second program verify levels.

Claim 6 **(Previously Presented)**: The method of claim 1, wherein (100%-X%) of the

program verify level is a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

Claim 7 **(Previously Presented)**: The method of claim 1, wherein the at least one flash memory cell of the group is contained within a page of the array.

Claim 8 **(Previously Presented)**: The method of claim 7, wherein the page of the array is situated between V_{SS} (source bias voltage) lines and between drain bit line junctions.

Claim 9 **(Previously Presented)**: The method of claim 1, further comprising:

storing a respective address of each flash memory cell of the group in a page buffer.

Claim 10 **(Currently Amended)**: A system for programming a group of at least one flash memory cell of an array, comprising:

means for performing a first pass of program verify and programming steps until each flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level after the first pass is completed; and

means for performing, after the first pass is completed, a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level.

Claim 11 **(Previously Presented)**: The system of claim 10, wherein the means for performing the first pass comprises:

means for determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step; and

means for generating a programming pulse for the flash memory cell of the group that has not attained substantially X% of the program verify level, during the programming step.

Claim 12 **(Previously Presented)**: The system of claim 10, wherein the means for performing the second pass comprises:

means for determining whether a flash memory cell of the group has not attained substantially the program verify level, during the program verify step; and

means for generating a programming pulse for the flash memory cell of the group that has not attained the program verify level, during the programming step.

Claim 13 **(Previously Presented)**: The system of claim 10, wherein the group includes a plurality of flash memory cells to be programmed to multi-level threshold voltages, the system further comprising:

means for performing the first pass of program verify and programming steps until each flash memory cell of a first sub-group of the group attains a threshold voltage that is at least Y% of a first program verify level but less than the first program verify level, and until each flash memory cell of a second sub-group of the group attains a threshold voltage that is at least Z% of a second program verify level but less than the second program verify level; and

means for performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second

program verify level.

Claim 14 **(Previously Presented)**: The system of claim 13, wherein (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to a higher of the first and second program verify levels.

Claim 15 **(Previously Presented)**: The system of claim 10, wherein (100%-X%) of the program verify level is a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

Claim 16 **(Previously Presented)**: The system of claim 10, wherein the at least one flash memory cell of the group is contained within a page of the array.

Claim 17 **(Previously Presented)**: The system of claim 16, wherein the page of the array is situated between V_{SS} (source bias voltage) lines and between drain bit line junctions.

Claim 18 **(Previously Presented)**: The system of claim 10, further comprising:

a page buffer for storing a respective address of each flash memory cell of the group.